Engineer's notebook

Low-cost processor package programs E-PROMs

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A problem for designers of the one-of-a-kind microprocessor-based system is the costly programming unit for the system's erasable-programmable read-only memories. Described here is an inexpensive E-PROM programmer built around a single-board microcomputer training kit, Intel's SDK-85. The scheme, used to achieve low-cost programming, can be readily generalized to other microcomputer systems.

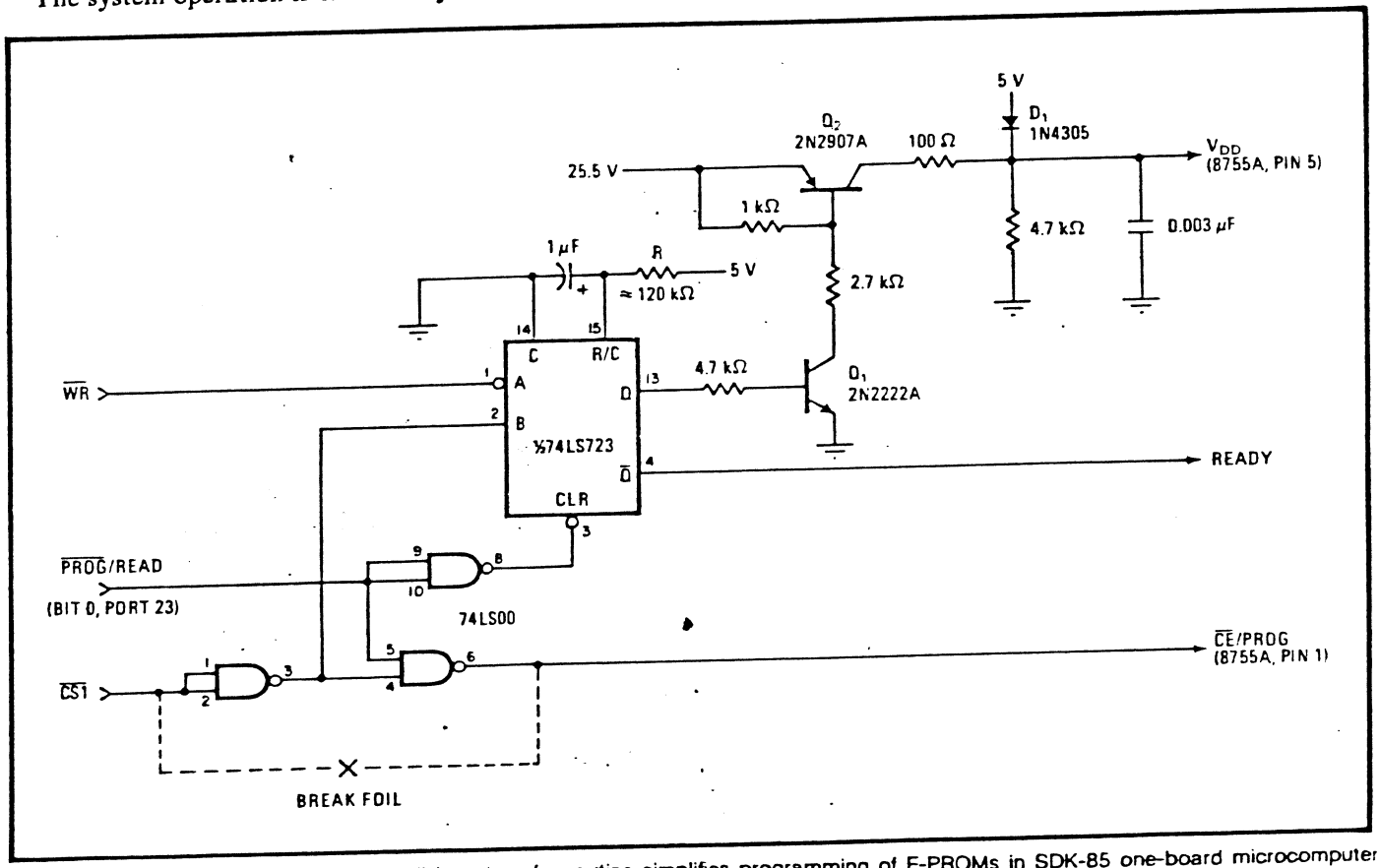
The SDK-85 uses the popular 8085 microprocessor as the central processing unit. The system has 2 kilobytes of read-only memory and 256 bytes of random-access memory. There is also a fully wired location for an additional 8355 ROM or 8755A E-PROM. With a few components and appropriate software, the added E-PROM can be programmed.

The system operation is clarified by observation of the schematic and the memory-byte transfer program. The memory-write signal ($\overline{WR}$) generated during the execution of the STAX B instruction is normally used to write data into a read/write memory. But here the signal triggers a 50-millisecond one-shot that pulses pin V_{DD} of the 8755A to 25 volts. Thus data on the system's data bus can be transferred into the addressed memory location. The address itself is automatically latched in an earlier machine cycle of the STAX B instruction.

The execution time of the STAX B instruction is extended to 50 ms by use of the CPU's READY line. Normally the READY line is used by slow memories to generate a wait state during a memory read/write cycle. In this application, the $\overline{WR}$ signal generated by the STAX B instruction triggers the 74123 one-shot, whose $\overline{Q}$ output stretches the $\overline{WR}$ signal by dropping the READY line for 50 ms.

The one-shot also turns on transistors Q_1 and Q_2, thus placing 25 volts on pin V_{DD}. When Q_1 and Q_2 are off, V_{DD} returns to a logic 1 state because of the action of pull-up diode D_1. This state satisfies the logic requirements of the V_{DD} pin during the READ mode.

The only modification of the SDK-85 circuit board required is to break the foil pattern at the $\overline{CE}$/PROG pin of the expansion ROM socket. The insertion of gating



Loading up. Minimal hardware and small byte-transfer routine simplifies programming of E-PROMs in SDK-85 one-board microcomputer design kit. Given starting and ending addresses of RAM data to be transferred, low-cost package programs 1 byte of E-PROM on each pass, then checks for parity at termination of run. If run terminates prematurely, E-PROM location causing fault will be displayed in register BC.

8085 BYTE-TRANSFER PROGRAM

```
        MVI A, 0CH      ; define port 23 as output port
        OUT 20H
        LXI B, PRMAD    ; load EPROM beginning address
        LXI H, SRTAD    ; load RAM beginning address
        LXI D, ENDAD    ; load RAM ending address
PROG:   XRA A           ; set in PROGRAM mode
        OUT 23H
        MOV A,M         ; get byte from RAM
        STAX B          ; program byte into EPROM
        MVI A, 01H      ; set in READ mode
        OUT 23H
        LDAX B          ; get byte from EPROM
        CMP M           ; check against RAM
        JNZ END         ; if error, jump to END
        MOV A,E         ; check if (DE) = (HL). If so, programming finished
        CMP L
        JNZ NEXT
        MOV A,D
        CMP H
        JZ END
NEXT:   INX H           ; not finished, program next byte
        INX B
        JMP PROG
END:    RST 1           ; return to monitor
```

circuits allows control over the chip-select signal $\overline{CS}$ routed to this pin. The $\overline{CS}_1$ signal should be gated to $\overline{CE}$/PROG during the read mode, while a logic 1 should be placed on this pin during the program mode.

Bit 0 of port 23 of the SDK-85 controls the mode; placed at logic 1, it puts the unit—otherwise in the program mode—in the read mode. The one-shot is then triggered by the falling edge of the $\overline{WR}$ pulse only when $\overline{CS}_1$ is active and the system is in the program mode.

The program itself is straightforward. A byte of the E-PROM is programmed and checked on each pass through the loop. The starting and ending addresses of the block of RAM to be transferred to the E-PROM are placed in the HL and DE register pairs, respectively. The BC register pair is then loaded with the starting address, and the RST 1 instruction returns control to a starting routine in the monitor. This routine saves the contents of all registers and flags.

Examination of the registers after program termination must show the contents of HL and DE to be equal. If not, the BC pair will contain the address of the E-PROM location that failed to program properly. □

Sharing floppy-disk bank increases processors' efficiency

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This interface unites two asynchronously operating 8080A microprocessors and four floppy-disk memories with a single floppy-disk controller. The scheme saves the cost of duplicating floppy-disk drives in a distributed processing environment.

With small business machines and others that may use the 8080 and operate in two modes concurrently—batch and data acquisition—entering data slows the batch