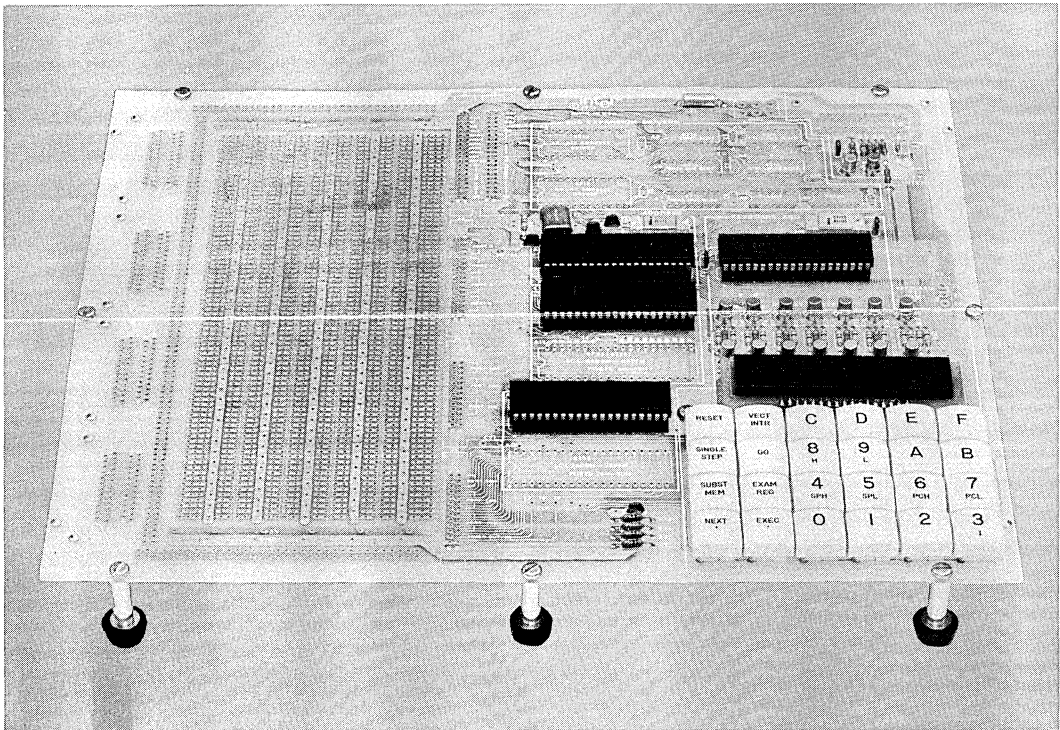




SDK-85 MCS-85™ SYSTEM DESIGN KIT

- Complete Single Board Microcomputer System Including CPU, Memory, and I/O
- Easy to Assemble, Low Cost, Kit Form
- Extensive System Monitor Software in ROM
- Interactive LED Display and Keyboard
- Large Wire-Wrap Area for Custom Interfaces
- Popular 8080A Instruction Set
- Interfaces Directly with TTY
- High Performance 3 MHz 8085A CPU (1.3 μ s Instruction Cycle)
- Comprehensive Design Library Included

The SDK-85 MCS-85 System Design Kit is a complete single board microcomputer system in kit form. It contains all components required to complete construction of the kit, including LED display, keyboard, resistors, caps, crystal, and miscellaneous hardware. Included is a preprogrammed ROM containing a system monitor for general software utilities and system diagnostics. The complete kit includes a 6-digit LED display and a 24-key keyboard for a direct insertion, examination, and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal. The SDK-85 is an inexpensive, high performance prototype system that has designed-in flexibility for simple interface to the user's application.



FUNCTIONAL DESCRIPTION

The SDK-85 is a complete 8085A microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, capacitors, and sockets are included. Assembly time varies from three to five hours, depending on the skill of the user. The SDK-85 functional block diagram is shown in Figure 1.

8085A Processor

The SDK-85 is designed around Intel's 8085A microprocessor. The Intel 8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software upward compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085A (CPU), 8156 (RAM), and 8355/8755 (ROM/PROM). A block diagram of the 8085A microprocessor is shown in Figure 2.

System Integration — The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

Addressing — The 8085A uses a multiplexed data bus. The 16-bit address is split between the 8-bit address bus and the 8-bit address/data bus. The on-chip address latches of 8155/8156/8355/8755 memory products allows a direct interface with the 8085A.

System Monitor

A compact but powerful system monitor is supplied with the SDK-85 to provide general software utilities and system diagnostics. It comes in a pre-programmed ROM.

Communications Interface

The SDK-85 communicates with the outside world through either the on-board LED display/keyboard combination, or the user's TTY terminal (jumper selectable).

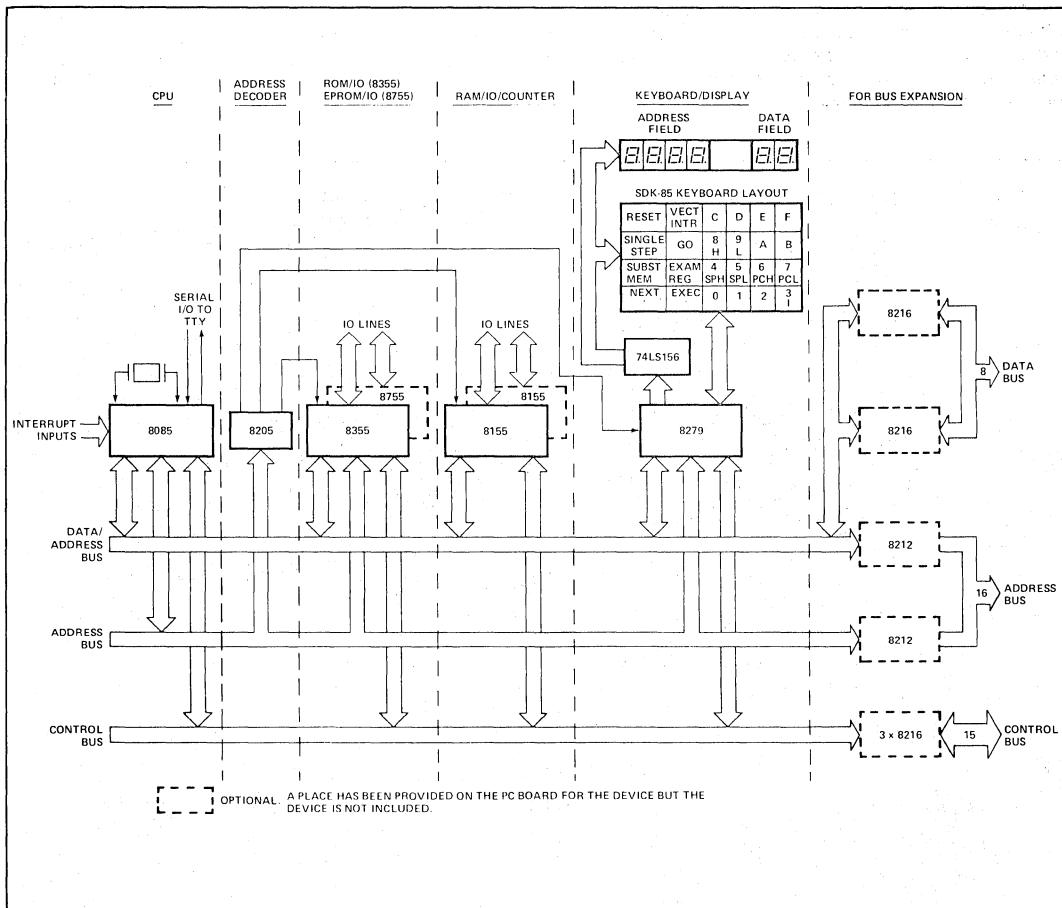


Figure 1. SDK-85 System Design Kit Functional Block Diagram

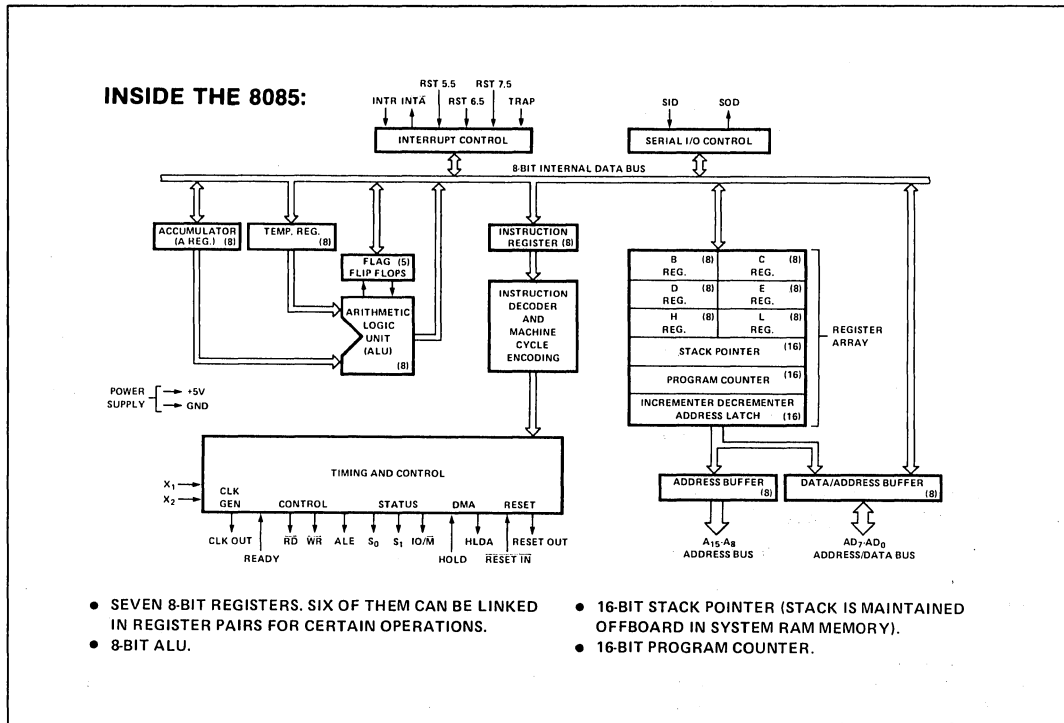


Figure 2. 8085A Microprocessor Block Diagram

Both memory and I/O can be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (45 sq. in.) is laid out as general purpose wire-wrap for the user's custom interfaces.

Commands — Keyboard monitor commands and teletype monitor commands are provided in Table 1 and Table 2 respectively.

Assembly

Only a few simple tools are required for assembly; soldering iron, cutters, screwdriver, etc. The SDK-85 user's manual contains step-by-step instructions for easy assembly without mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-85 is ready to go. The monitor starts immediately upon power-on or reset.

Table 1. Keyboard Monitor Commands

Command	Operation
Reset	Starts monitor.
Go	Allows user to execute user program.
Single step	Allows user to execute user program one instruction at a time—useful for debugging.
Substitute memory	Allows user to examine and modify memory locations.
Examine register	Allows user to examine and modify 8085A's register contents.
Vector interrupt	Serves as user interrupt button.

Table 2. Teletype Monitor Commands

Command	Operation
Display memory	Displays multiple memory locations.
Substitute memory	Allows user to examine and modify memory locations one at a time.
Insert instructions	Allows user to store multiple bytes in memory.
Move memory	Allows user to move blocks of data in memory.
Examine register	Allows user to examine and modify the 8085A's register contents.
Go	Allows user to execute user programs.

Documentation

In addition to detailed information on using the monitors, the SDK-85 user's manual provides circuit diagrams, a monitor listing, and a description of how the system works. The complete design library for the SDK-85 is shown in Figure 7-11 and listed in the Specifications section under Reference Manuals.



Figure 3. SDK-85 Design Library

8085A INSTRUCTION SET

Table 3 contains a summary of processor instructions used for the 8085A microprocessor.

Table 3. Summary of 8085A Processor Instructions

Mnemonic ¹	Description	Instruction Code ²								Clock ³ Cycles	Mnemonic ¹	Description	Instruction Code ²								Clock ³ Cycles			
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
MOVE, LOAD, AND STORE																								
MOV r1r2	Move register to register	0	1	D	D	D	S	S	S	4	LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10			
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7	INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6			
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7	DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6			
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7	JUMP													
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10	JMP	Jump unconditional	1	1	0	0	0	0	1	1	10			
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10	JC	Jump on carry	1	1	0	1	0	1	0	1	7/10			
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10	JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10			
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10	JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10			
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7	JNZ	Jump on no zero	1	1	0	0	0	1	0	7/10				
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7	JP	Jump on positive	1	1	1	0	0	0	1	0	7/10			
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7	JM	Jump on minus	1	1	1	1	1	0	1	0	7/10			
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7	JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10			
STA	Store A direct	0	0	1	1	0	0	1	0	13	JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10			
LDA	Load A direct	0	0	1	1	1	0	1	0	13	PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6			
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16	CALL													
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16	CALL	Call unconditional	1	1	0	0	1	1	0	1	18			
XCHG	Exchange D & E, H & L registers	1	1	1	0	1	0	1	1	4	CC	Call on carry	1	1	0	1	1	1	0	0	9/18			
STACK OPS																								
PUSH B	Push register pair B & C on stack	1	1	0	0	0	1	0	1	12	CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18			
PUSH D	Push register, pair D & E on stack	1	1	0	1	0	1	0	1	12	CZ	Call on zero	1	1	0	0	1	1	0	0	9/18			
PUSH H	Push register pair H & L on stack	1	1	1	0	0	1	0	1	12	CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18			
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12	CP	Call on positive	1	1	1	1	0	1	0	0	9/18			
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10	CM	Call on minus	1	1	1	1	1	1	0	0	9/18			
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10	CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18			
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10	CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18			
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	RETURN													
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	16	RET	Return	1	1	0	0	1	0	0	1	10			
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6	RC	Return on carry	1	1	0	1	1	0	0	0	6/12			
														RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
														RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
														RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
														RP	Return on positive	1	1	1	1	0	0	0	0	6/12
														RM	Return on minus	1	1	1	1	1	0	0	0	6/12

continued

SDK-85

Table 3. Summary of 8085A Processor Instructions (Continued)

Mnemonic ¹	Description	Instruction Code ²								Clock ³ Cycles	Mnemonic ¹	Description	Instruction Code ²								Clock ³ Cycles					
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀						
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12	LOGICAL															
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12	ANA r	And register with A	1	0	1	0	0	S	S	S	4					
RESTART											XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4					
RST	Restart	1	1	A	A	A	1	1	1	12	ORA r	Or register with A	1	0	1	1	0	S	S	S	4					
INCREMENT AND DECREMENT											CMP r	Compare register with A	1	0	1	1	1	S	S	S	4					
INR r	Increment register	0	0	D	D	D	1	0	0	4	ANA M	And memory with A	1	0	1	0	0	1	1	0	7					
DCR r	Decrement register	0	0	D	D	D	1	0	1	4	XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7					
INR M	Increment memory	0	0	1	1	0	1	0	0	10	ORA M	Or memory with A	1	0	1	1	0	1	1	0	7					
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7					
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6	ANI	And immediate with A	1	1	1	0	0	1	1	0	7					
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6	XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7					
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6	ORI	Or immediate with A	1	1	1	1	0	1	1	0	7					
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6	CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7					
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6	ROTATE															
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6	RLC	Rotate A left	0	0	0	0	0	1	1	1	4					
ADD											RRC	Rotate A right	0	0	0	0	1	1	1	1	4					
ADD r	Add register to A	1	0	0	0	0	S	S	S	4	RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4					
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4	RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4					
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	SPECIALS															
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	CMA	Complement A	0	0	1	0	1	1	1	1	4					
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7	STC	Set carry	0	0	1	1	0	1	1	1	4					
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	CMC	Complement carry	0	0	1	1	1	1	1	1	4					
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10	DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4					
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10	INPUT/OUTPUT															
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10	IN	Input	1	1	0	1	1	0	1	1	10					
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10	OUT	Output	1	1	0	1	0	0	1	1	10					
SUBTRACT											CONTROL															
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4	EI	Enable interrupts	1	1	1	1	1	0	1	1	4					
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4	DI	Disable interrupts	1	1	1	0	0	1	1	4						
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	NOP	No-operation	0	0	0	0	0	0	0	4						
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	HLT	Halt	0	1	1	1	0	1	1	0	5					
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7	NEW 8085 INSTRUCTIONS															
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	RIM	Read interrupt mask	0	0	1	0	0	0	0	0	4					
											SIM	Set interrupt mask	0	0	1	1	0	0	0	0	4					

Notes

1. All mnemonics copyright © Intel Corporation 1977.
2. DDD or SSS: B=000, C=001, D=010, E=011, H=100, L=101, Memory=110, A=111.
3. Two possible cycle times. (6/12) indicates instruction cycles dependent on condition flags.

SPECIFICATIONS

Central Processor

CPU — 8085A

Instruction Cycle — 1.3 μs

Tcy — 330 ns

Memory

ROM — 2K bytes (expandable to 4K bytes) 8355/8755A

RAM — 256 bytes (expandable to 512 bytes) 8155

Addressing

ROM — 0000-07FF (expandable to 0FFF with an additional 8355/8755A)

RAM — 2000-20FF (2800-28FF available with an additional 8155)

Note

The wire-wrap area of the SDK-85 PC board may be used for additional custom memory expansion up to the 64K-byte addressing limit of the 8085A.

Input/Output

Parallel — 38 lines (expandable to 76 lines)
Serial — Through SID/SOD ports of 8085A. Software generated baud rate.
Baud Rate — 110

Interfaces

Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Serial I/O — 20 mA current loop TTY

Note
 By populating the buffer area of the board, the user has access to all bus signals that enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts

Three Levels
 (RST 7.5) — Keyboard interrupt
 (RST 6.5) — TTL input
 (INTR) — TTL input

DMA

Hold Request — Jumper selectable. TTL compatible input.

Software

System Monitor — Pre-programmed 8755A or 8355 ROM
Addresses — 0000-07FF
Monitor I/O — Keyboard/display or TTY (serial I/O)

Physical Characteristics

Width — 12.0 in. (30.5 cm)
Height — 10 in. (25.4 cm)
Depth — 0.50 in. (1.27 cm)
Weight — approx. 12 oz

Electrical Characteristics

DC Power Requirement (power supply not included in kit)

Voltage	Current
V _{CC} 5V ± 5%	1.3A
V _{TTY} - 10V ± 10%	0.3A
	(V _{TTY} required only if teletype is connected)

Environmental Characteristics

Operating Temperature — 0-55 °C

Reference Manuals

9800451 — SDK-85 User's Manual (SUPPLIED)
9800366 — MCS-85 User's Manual (SUPPLIED)
9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)
8085/8080 Assembly Language Reference Card (SUPPLIED)
 Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

SDK-85 MCS-85 system design kit